In the Claims

CLAIMS

Claims 1-40 (Canceled).

41. (Previously presented) An integrated circuit device comprising:

a semiconductor die comprising synchronous-link dynamic random access memory circuitry;

a heat sink thermally coupled with the semiconductor die; and

a housing encapsulating at least a portion of the heat sink and positioned between substantially an entirety of the heat sink and semiconductor die.

42. (Previously presented) The integrated circuit device according to claim 41 further comprising at least one lead coupled with the semiconductor die and the housing encapsulates at least a portion of the at least one lead.

43. (Previously presented) The integrated circuit device according to claim 41 wherein the heat sink comprises:

a body; and

at least one lead coupled with the body and configured to dissipate heat from the semiconductor die externally of the housing.

44. (Previously presented) The integrated circuit device according to claim 43 wherein the housing encapsulates at least a portion of the at least one lead.

45. (Previously presented) The integrated circuit device according to claim 41 wherein the housing encapsulates substantially an entirety of the heat sink.

46. (Previously presented) The integrated circuit device according to claim 41 wherein the housing surrounds the heat sink and the semiconductor die.

47. (Previously presented) The integrated circuit device according to claim 41 wherein the housing encapsulates the semiconductor die.

48. (Previously presented) An integrated circuit device comprising:

a housing enclosing a semiconductor die comprising memory circuitry; and

a heat sink positioned in heat-receiving relation with the semiconductor die and comprising leads extending outward of the housing and configured to release heat outside the housing.

49. (Previously presented) The integrated circuit device according to claim 48 wherein the heat sink comprises at least one lead configured to conduct heat externally of the housing.

50. (Previously presented) The integrated circuit device according to claim 48 wherein the housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

51. (Previously presented) The integrated circuit device according to claim 48 wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and at least partially enclosing the heat sink.

52. (Previously presented) The integrated circuit device according to claim 48 wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and the heat sink.

53. (Previously presented) An integrated circuit device comprising:

a first lead frame;

a semiconductor die secured to the first lead frame;

a second lead frame comprising a heat sink thermally coupled with the semiconductor die; and

a housing formed about at least portions of the semiconductor die and heat sink.

54. (Previously presented) The integrated circuit device according to claim 53 wherein the housing comprises an encapsulant housing.

55. (Previously presented) The integrated circuit device according to claim 53 wherein the semiconductor die comprises memory circuitry.

56. (Previously presented) The integrated circuit device according to claim 53 wherein the housing is configured to provide portions of the first lead frame and second lead frame outwardly exposed relative to the housing.

57. (Previously presented) The integrated circuit device according to claim 56 wherein the housing comprises a plurality of sides, and wherein the portions of the first and second lead frames extend from the same side.

58. (Previously presented) The integrated circuit device according to claim 53 wherein the portions of the first and second lead frames are bent to provide horizontal mounting of the integrated circuit device.

59. (Previously presented) The integrated circuit device according to claim 53 wherein the housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

60. (Previously presented) The integrated circuit device according to claim 53 wherein the housing encapsulates an entirety of the semiconductor die.

61. (Previously presented) The integrated circuit device according to claim 53 wherein the housing encapsulates an entirety of the semiconductor die and the heat sink.

62. (Previously presented) The integrated circuit device according to claim 53 wherein the heat sink comprises leads.

63. (Previously presented) an integrated circuit device comprising:

a semiconductor die including a first lead;

a heat sink comprising a second lead and thermally coupled with the semiconductor die; and

a housing encapsulating the heat sink and semiconductor die, wherein at least portions of the first and second leads contact a common surface of the housing.

64. (Previously presented) the integrated circuit device according to claim 63 wherein the first lead terminates in a first direction and the second lead terminates in a second direction different from the first direction.

65. (Previously presented) The integrated circuit device according to claim 63 wherein the at least the portion of the first lead comprises an angle.

66. (Previously presented) The integrated circuit device according to claim 63 wherein the at least the portion of the first lead extends outwardly of the housing from the common surface.

67. (Previously presented) The integrated circuit device according to claim 63 wherein the at least the portions of the first and second leads extend outwardly of the housing from the common surface.

68. (Previously presented) The integrated circuit device according to claim 63 wherein the at least the portion of the first lead comprises at least two angles.

69. (Previously presented) an integrated circuit device comprising:

a housing enclosing a semiconductor die comprising memory circuitry;

a heat sink positioned in heat-receiving relation with the semiconductor die and configured to release heat outside the housing; and

wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and at least partially enclosing the heat sink.

70. (Previously presented) An integrated circuit device comprising:

a housing enclosing a semiconductor die comprising memory circuitry;

a heat sink positioned in heat-receiving relation with the semiconductor die and configured to release heat outside the housing; and

wherein the housing comprises a first housing enclosing the semiconductor die and a second housing enclosing the first housing and the heat sink.